



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,457	02/12/2004	Marco Pasotti	S1022.81104US00	2275
23628	7590	01/19/2006		
WOLF GREENFIELD & SACKS, PC FEDERAL RESERVE PLAZA 600 ATLANTIC AVENUE BOSTON, MA 02210-2211			EXAMINER PHAN, TRONG Q	
			ART UNIT 2827	PAPER NUMBER

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,457	PASOTTI ET AL.	
	Examiner	Art Unit	
	TRONG PHAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 November 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pollachek, 4,648,074, in view of Lee et al., 5,909,405, Garni et al., 6,621,729, and Passotti et al., 6,535,428.

Pollachek, 4,648,074, discloses in Fig. 3 a NAND-stack of read only memory (ROM) device (see lines 24-27, column 1) comprising:

Regarding claims 1, 4-6, 9, 11-13, 19-22, 26 and 30-32

memory cell array 30;

reference memory cell array 31;

differential amplifier 22 which reads on the output comparator as recited in claims 1, 11 and 26;

first load PMOS transistor PTR for connection between supply terminal VDD and an input terminal of differential amplifier 22 and being connected to reference cell array 31;

second load PMOS transistor PT1;

a control circuit (not shown) for providing the precharge PC to the control gate electrode of both first and second PMOS transistors PT1 and PTR;

a plurality of sense amplifiers, as shown in Fig. 5, which read on the read/write circuit as recited in claim 12; wherein:

the operating power supply voltage VDD, for example, 5 volts (see lines 60-61, column 3), which is for example, therefore, it can be low less than 1.5 volts as recited in claims 30-31 depending the design operating parameters for the device as well as the size of the PMOS load transistors as well known in the art; or when depletion PMOS transistor being used, the low power supply voltage VDD of less than 1.5 volts as recited in claims 30-31 will be applied since the threshold voltage of depletion PMOS transistors being of -6 volts for logic "1" and -3 volts for logic "0" (see lines 38-63, column 9) NMOS transistors could also be used instead of PMOS transistors with appropriate care for the polarity of operating potential (see lines 64-68, column 9).

What is not shown in Figs. 3 and 5 of Pollachek, 4,648,074, is the nonvolatile memory cell as recited in claims 1, 4-6, 9, 11-13, 19-22, 26 and 30-32.

Lee et al., 5,909,405, discloses the teaching that NAND-type read only memory is referred to as nonvolatile memory (see lines 11-14, column 1).

In view of Lee et al., 5,909,405, the NAND-stack of read only memory (ROM) device in Figs. 3 and 5 of Pollachek, 4,648,074, is obviously a nonvolatile memory device.

What is not shown in Figs. 3 and 5 of Pollachek, 4,648, 074, which is modified

by Lee et al., 5,908,405, is the feedback amplifier as recited in claims 2-3, 7, 10, 14-18 and 23-27.

Garni et al., 6,621,729, discloses in Fig. 1 the teaching of using feedback operational amplifier 12 having a first input connected to the drain of PMOS load transistor 14 and a second input connected to a reference voltage VREF which can be a bandgap voltage as well known in the art .

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the present invention was made to utilize the feedback operational amplifier 12 in Fig. 1 of Garni et al., 6,621,729, for providing bias voltage (see lines 20-22, column 2 of Garni et al., 6,621,729) to the control gates of both load PMOS transistors PT and PTR in Figs 3 and 5 of Pollachek, 4,648,074.

One of ordinary skill in the art also would have known to utilize two feedback operational amplifiers 12 in Fig. 1 of Garni et al., 6,621,729, for provide the bias voltage separately to each of control gates of load PMOS transistors PT and PTR in Figs 3 and 5 of Pollachek, 4,648,074, as recited in claim 23.

What is not shown in Figs. 3 and 5 of Pollachek, 4,648,074, which is modified by Lee et al., 5,908,405, and Garni et al., 6,621,729, is the first and second voltage limiters as recited in claim 8 which either limiter comprising a third transistor having an inverter coupled to a gate and a conducting terminal as recited in claim 29.

Pasotti et al., 6,535,428, discloses in Fig. 1 the teaching of using NMOS transistors MN1 connecting load MP1 and memory cells MC and NMOS transistor MN2 connecting between load transistor MP2 and reference memory cells CR. Also,

as shown in Fig. 2, each of NMOS transistors MN1 and MN2 is controlled by a feedback inverter INV1 (it should be noted that Fig. 2 does show only circuit branch 11 (see lines 59-65, column 8).

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the present invention was made to utilize a first set of NMOS transistor MN1 and inverter INV for connecting between PMOS load transistor PT and memory cells 30 and a second set of NMOS transistor MN1 and inverter INV for connecting between PMOS load transistor PTR and reference memory cells 31 in Figs. 3 and 5 of Pollachek, 4,648,074, which is modified by Lee et al., 5,908,405, and Garni et al., 6,621,729, for the purpose of keeping the drain voltage of the memory cells 30 as well as the drain voltage of the reference memory cells 31 in Figs. 3 and 5 of Pollachek, 4,648,074, as a predetermined value (see lines 10-24, column 5 of Pasotti et al., 6,535,428) such as the first and second voltage limiters as recited in claims 8 and 29.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Response to Arguments

4. Applicant's arguments with respect to claims 1-32 have been considered but are moot in view of the new ground(s) of rejection.

In view of the feature "a first load for connection between a supply terminal and an input terminal of an output comparator" as newly added to independent claim 1 and the addition of new claims 13-32 without canceling the rejected claims, the last office action of 7/7/05 has been withdrawn. A necessitated new ground of rejection has been set forth and made FINAL as above.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (571) 272-1794. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on (571)272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

Art Unit: 2827

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).


TRONG PHAN
PRIMARY EXAMINER